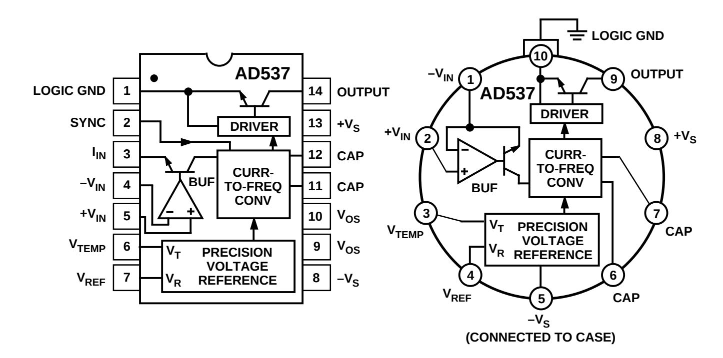


Integrated Circuit Voltage-to-Frequency Converter

AD537*

FEATURES
- **Low Cost A-D Conversion**
- **Versatile Input Amplifier**
  - **Positive or Negative Voltage Modes**
  - **Negative Current Mode**
  - **High Input Impedance, Low Drift**
- **Single Supply, 5 V to 36 V**
- **Linearity: ±0.05% FS**
- **Low Power: 1.2 mA Quiescent Current**
- **Full-Scale Frequency up to 100 kHz**
- **1.00 V Reference**
- **Thermometer Output (1 mV/K)**
- **F-V Applications**
- **MIL-STD-883 Compliant Versions Available**

PIN CONFIGURATIONS
"D" Package (TO-116) **"H" Package (TO-100)**



PRODUCT DESCRIPTION

The AD537 is a monolithic V-F converter consisting of an input amplifier, a precision oscillator system, an accurate internal reference generator and a high current output stage. Only a single external RC network is required to set up any full-scale (F.S.) frequency up to 100 kHz and any F.S. input voltage up to ±30 V. Linearity error is as low as ±0.05% for 10 kHz F.S., and operation is guaranteed over an 80 dB dynamic range. The overall temperature coefficient (excluding the effects of external components) is typically ±30 ppm/°C. The AD537 operates from a single supply of 5 V to 36 V and consumes only 1.2 mA quiescent current.

A temperature-proportional output, scaled to 1.00 mV/K, enables the circuit to be used as a reliable temperature-to-frequency converter; in combination with the fixed reference output of 1.00 V, offset scales such as 0°C or 0°F can be generated.

The low drift (1 μV/°C typ) input amplifier allows operation directly from small signals (e.g., thermocouples or strain gages) while offering a high (250 MΩ) input resistance. Unlike most V–F converters, the AD537 provides a square-wave output, and can drive up to 12 TTL loads, LEDs, very long cables, etc.

The excellent temperature characteristics and long-term stability of the AD537 are guaranteed by the primary bandgap reference generator and the low T.C. silicon chromium thin film resistors used throughout.

The device is available in either a TO-116 ceramic DIP or a TO-100 metal can; both are hermetically sealed packages.

***Protected by Patent Nos. 3,887,963 and RE 30,586.**

The AD537 is available in three performance/temperature grades; the J and K grades are specified for operation over the 0°C to +70°C range while the AD537S is specified for operation over the extended temperature range, –55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD537 is a complete V-F converter requiring only an external RC timing network to set the desired full-scale frequency and a selectable pull-up resistor for the open collector output stage. Any full-scale input voltage range from 100 mV to 10 volts (or greater, depending on $+V_S$) can be accommodated by proper selection of timing resistor. The full-scale frequency is then set by the timing capacitor from the simple relationship, f = V/10RC.
2. The power supply requirements are minimal, only 1.2 mA quiescent current is drawn from a single positive supply from 4.5 volts to 36 volts. In this mode, positive inputs can vary from 0 volts (ground) to ($+V_S$ – 4) volts. Negative inputs can easily be connected for below ground operation.
3. F-V converters with excellent characteristic are also easy to build by connecting the AD537 in a phase-locked loop. Application particulars are shown in Figure 6.
4. The versatile open-collector NPN output stage can sink up to 20 mA with a saturation voltage less than 0.4 volts. The Logic Common terminal can be connected to any level between ground (or $–V_S$) and 4 volts below $+V_S$. This allows easy direct interface to any logic family with either positive or negative logic levels.
5. The AD537 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Product Databook or current AD537/883B data sheet for detailed specifications.

REV. B

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AD537–SPECIFICATIONS (typical @ +25°C with V_S (total) = 5 V to 36 V, unless otherwise noted)

Model	AD537JH	AD537JD	AD537KD AD537KH	AD537SD[1] AD537SH[1]
CURRENT-TO-FREQUENCY CONVERTER				
Frequency Range	0 kHz to 150 kHz	*	*	*
Nonlinearity[1]				
f_{MAX} = 10 kHz	0.15% max (0.1% typ)	*	0.07% max	**
f_{MAX} = 100 kHz	0.25% max (0.15% typ)	*	0.1% max	**
Full-Scale Calibration Error				
C = 0.01 µF, I_{IN} = 1.000 mA	±10% max	±7% max	±5% max	**
vs. Supply (f_{MAX} < 100 kHz)	±0.1%/V max (0.01% typ)	*	*	*
vs. Temp (T_{MIN} to T_{MAX})	±150 ppm/°C max (50 ppm typ)	*	50 ppm/°C max (30 ppm typ)[2]	250 ppm/°C max
ANALOG INPUT AMPLIFIER				
(Voltage-to-Current Converter)				
Voltage Input Range				
Single Supply	0 to ($+V_S$ – 4) Volts (min)	*	*	*
Dual Supply	$–V_S$ to ($+V_S$ – 4) Volts (min)	*	*	*
Input Bias Current				
(Either Input)	100 nA	*	*	*
Input Resistance (Noninverting)	250 MΩ	*	*	*
Input Offset Voltage				
(Trimmable in "D" Package Only)	5 mV max	*	2 mV max	**
vs. Supply	200 µV/V max	100 µV/V max	100 µV/V max	**
vs. Temp (T_{MIN} to T_{MAX})	5 µV/°C	*	1 µV/°C	10 µV/°C max
Safe Input Voltage[3]	$±V_S$	*	*	*
REFERENCE OUTPUTS				
Voltage Reference				
Absolute Value	1.00 Volt ± 5% max	*	*	*
vs. Temp (T_{MIN} to T_{MAX})	50 ppm/°C	*	100 ppm/°C max	**
vs. Supply	±0.03%/V max	*	*	*
Output Resistance[4]	380 Ω	*	*	*
Absolute Temperature Reference[5]				
Nominal Output Level	1.00 mV/K	*	*	*
Initial Calibration @ +25°C	298 mV (±5 mV)	*	298 mV (±5 mV max)	**
Slope Error from 1.00 mV/K	±0.02 mV/K	*	*	*
Slope Nonlinearity	±0.1 K	*	*	*
Output Resistance[5]	900 Ω	*	*	*
OUTPUT INTERFACE (Open Collector Output)				
(Symmetrical Square Wave)				
Output Sink Current in Logic "0"				
V_{OUT} = 0.4 V max (T_{MIN} to T_{MAX})	20 mA min	20 mA min	20 mA min	10 mA min
Output Leakage Current in Logic "1"				
(T_{MIN} to T_{MAX})	200 nA max	*	*	2 µA max
Logic Common Level Range	$–V_S$ to ($+V_S$ – 4) Volts	*	*	*
Rise/Fall Times (C_T = 0.01 µF)				
I_{IN} = 1 mA	0.2 µs	*	*	*
I_{IN} = 1 µA	1 µs	*	*	*
POWER SUPPLY				
Voltage, Rated Performance				
Single Supply	4.5 V to 36 V	*	*	*
Dual Supply	±5 V to ±18 V	*	*	*
Quiescent Current	1.2 mA (2.5 mA max)	*	*	*
TEMPERATURE RANGE				
Rated Performance	0°C to +70°C	*	*	–55°C to +125°C
Storage	–65°C to +150°C	*	*	*
PACKAGE OPTIONS[6, 7]				
TO-116 Ceramic DIP (D-14)		AD537JD	AD537KD	AD537SD
TO-100 Header (H-10A)	AD537JH		AD537KH	AD537SH

NOTES
*Specifications same as AD537JH.
**Specifications same as AD537K.
[1]Nonlinearity is specified for a current input level (I_{IN}) to the converter from 0.1 µA to 1000 µA. Converter has 100% overrange capability up to I_{IN} = 2000 µA with slightly reduced linearity. Nonlinearity is defined as deviation from a straight line from zero to full scale, expressed as a percentage of full scale.
[2]Guaranteed not tested.
[3]Maximum voltage input level is equal to the supply on either input terminal. However, large negative voltage levels can be applied to the negative terminal if the input is scaled to a nominal 1 mA full scale through an appropriate value resistor (See Figure 2).
[4]Loading the 1.0 volt or 1 mV/K outputs can cause a significant change in overall circuit performance, as indicated in the applications section. To maintain normal operation, these outputs should be operated into the external buffer or an external amplifier.
[5]Temperature reference output performance is specified from 0°C to +70°C for "J" and "K" devices, –55°C to +125°C for "S" model.
[6]D = Ceramic DIP; H = Hermetic Metal Can. For outline information see Package Information section.
[7]For AD537/883B specifications, refer to *Analog Devices Military Products Databook*.
Specifications subject to change without notice.

CIRCUIT OPERATION

Block diagrams of the AD537 are shown above. A versatile operational amplifier (BUF) serves as the input stage; its purpose is to convert and scale the input voltage signal to a drive current in the NPN follower. Optimum performance is achieved when, at the full-scale input voltage, a 1 mA drive current is delivered to the current-to-frequency converter. The drive current to the current-to-frequency converter (an astable multivibrator) provides both the bias levels and the charging current to the externally connected timing capacitor. This "adaptive" bias scheme allows the oscillator to provide low nonlinearity over the entire current input range of 0.1 µA to 2000 µA. The square wave oscillator output goes to the output driver which provides a floating base drive to the NPN power transistor. This floating drive allows the logic interface to be referenced to a different level than $-V_S$. The "SYNC" input ("D" package only) allows the oscillator to be slaved to an external master oscillator; this input can also be used to shut off the oscillator.

The reference generator uses a bandgap circuit (this allows single-supply operation to 4.5 volts which is not possible with low T.C. Zeners) to provide the reference and bias levels for the amplifier and oscillator stages. The reference generator also provides the precision, low T.C. 1.00 volt output and the V_{TEMP} output which tracks absolute temperature at 1 mV/K.

V-F CONNECTION FOR POSITIVE INPUT VOLTAGES

The positive voltage input range is from $-V_S$ (ground in single supply operation) to 4 volts below the positive supply. The connection shown in Figure 1 provides a very high (250 MΩ) input impedance. The input voltage is converted to the proper drive current at Pin 3 by selecting a scaling resistor. The full-scale current is 1 mA, so, for example a 10 volt range would require a nominal 10 kΩ resistor. The trim range required will depend on capacitor tolerance. Full-scale currents other than 1 mA can be chosen, but linearity will be reduced; 2 mA is the maximum allowable drive.

As indicated by the scaling relationship in Figure 1, a 0.01 µF timing capacitor will give a 10 kHz full-scale frequency, and 0.001 µF will give 100 kHz with a 1 mA drive current. The maximum frequency is 150 kHz. Polystyrene or NPO ceramic capacitors are preferred for T.C. and dielectric absorption; polycarbonate or mica are acceptable; other types will degrade linearity. The capacitor should be wired very close to the AD537.

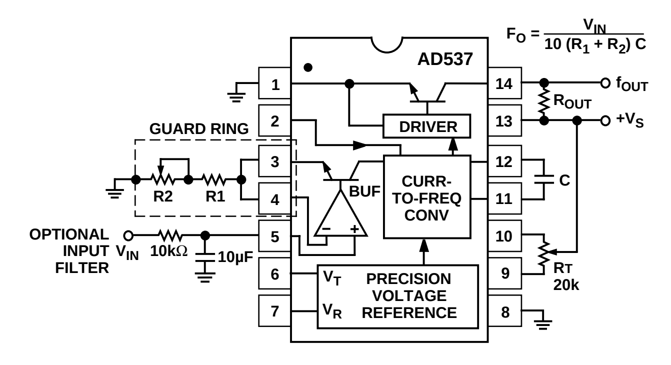


Figure 1. Standard V-F Connection for Positive Input Voltages

V-F CONNECTIONS FOR NEGATIVE INPUT VOLTAGE OR CURRENT

A wide range of negative input voltages can be accommodated with proper selection of the scaling resistor, as indicated in Figure 2. This connection, unlike the buffered positive connection, is not high impedance since the 1 mA F.S. drive current must be supplied by the signal source. However, very large negative voltages beyond the supply can be handled easily; just modify the scaling resistors appropriately. Diode CR1 (HP50822811) is necessary for overload and latchup protection for current or voltage inputs.

If the input signal is a true current source, R1 and R2 are not used. Full-scale calibration can be accomplished by connecting a 200 kΩ pot in series with a fixed 27 kΩ from Pin 7 to $-V_S$ (see calibration section, below).

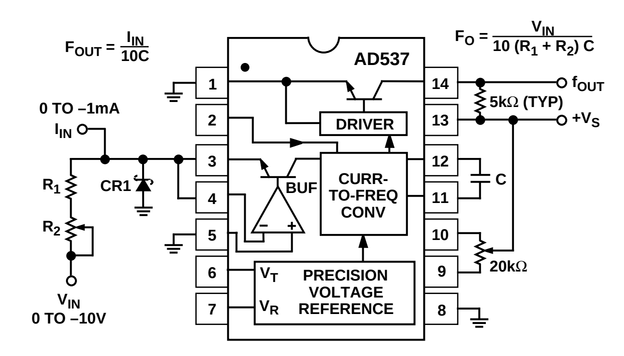


Figure 2. V-F Connections for Negative Input Voltage or Current

CALIBRATION

There are two independent adjustments: scale and offset. The first is trimmed by adjustment of the scaling resistor R and the second by the (optional) potentiometer connected to $+V_S$ and the V_{OS} pins ("D" package only). Precise calibration requires the use of an accurate voltage standard set to the desired FS value and a frequency meter; a scope is useful for monitoring output waveshape. Verification of linearity requires the availability of a switchable voltage source (or a DAC) having a linearity error below ±0.005%, and the use of long measurement intervals to minimize count uncertainties. *Every AD537 is automatically tested for linearity,* and it will not usually be necessary to perform this verification, which is both tedious and time-consuming.

Although drifts are small it is good practice to allow the operating environment to attain stable temperature and to ensure that the supply, source and load conditions are proper. Begin by setting the input voltage to 1/10,000 of full scale. Adjust the offset pot until the output frequency is 1/10,000 of full scale (for example 1 Hz for FS of 10 kHz). This is most easily accomplished using a frequency meter connected to the output. Then apply the FS input voltage and adjust the gain pot until the desired FS frequency is indicated. In applications where the FS input is small, this adjustment will very slightly affect the offset voltage, due to the input bias current of the buffer amplifier. A change of 1 kΩ in R will affect the input by approximately 100 µV, which is as much as 0.1% of a 100 mV FS range. Therefore, it may be necessary to repeat the offset and scale adjustments for the highest accuracy. The design of the input amplifier is such that the input voltage drift after offset nulling is typically below 1 µV/°C.

In some cases the signal may be in the form of a negative current source. This can be handled in a similar way to a negative input voltage. However, the scaling resistor is no longer required, eliminating the capability of trimming full scale in this fashion. Since it will usually be impractical to vary the capacitance, an alternative calibration scheme is needed. This is shown in Figure 3. A resistor-potentiometer connected from the V_R output to $-V_S$ will alter the internal operating conditions in a predictable way, providing the necessary adjustment range. With the values shown, a range of ±4% is available; a larger range can be attained by reducing R1. This technique does not degrade the temperature-coefficient of the converter, and the linearity will be as for negative input voltages. The minimum supply voltage may be used.

Unless it is required to set the input node at exactly ground potential, no offset adjustment is needed. The capacitor C is selected to be 5% below the nominal value; with R2 in its midposition the output frequency is given by:

$$f = \frac{I}{10.5 \times C}$$

where f is in kHz, I is in mA and C is in µF. For example, for a FS frequency of 10 kHz at a FS input of 1 mA, C = 9500 pF. Calibration is effected by applying the full-scale input and adjusting R2 for the correct reading.

This alternative adjustment scheme may also be used when it is desired to present an exact input resistance in the negative voltage mode. The scaling relationship is then

$$f = \frac{V}{R_{EXACT}} \times \frac{1}{10.5\,C}$$

The calibration procedure is then similar to that used for positive input voltages, except that the scale adjustment is by means of R2.

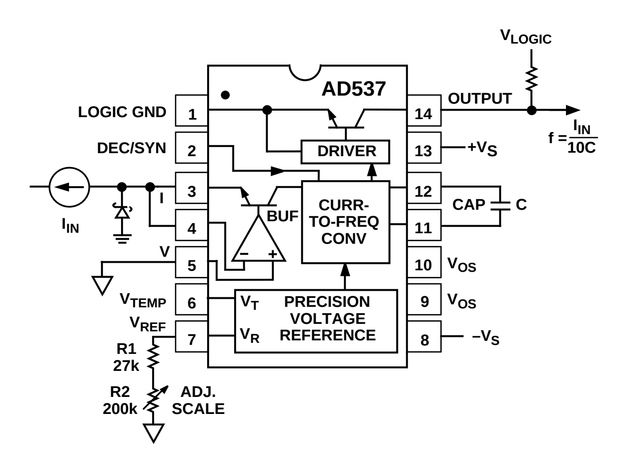


Figure 3. Scale Adjustment for Current Inputs

INPUT PROTECTION

The AD537 was designed to be used with a minimum of additional hardware. However, the successful application of a precision IC involves a good understanding of possible pitfalls and the use of suitable precautions.

The $-V_{IN}$, $+V_{IN}$ and I_{IN} pins should not be driven more than 300 mV below $-V_S$. This would cause internal junctions to conduct, possibly damaging the IC. The AD537 can be protected from "below $-V_S$" inputs by a Schottky diode, CR1 (HP5082-2811) as shown in Figure 3. It is also desirable not to drive $+V_{IN}$, $-V_{IN}$ and I_{IN} above $+V_S$. In operation, the converter will become very nonlinear for inputs above ($+V_S$ – 3.5 V). Control currents above 2 mA will also cause nonlinearity.

The 80 dB dynamic range of the AD537 guarantees operation from a control current of 1 mA (nominal FS) down to 100 nA (equivalent to 1 mV to 10 V FS). Below 100 nA improper operation of the oscillator may result, causing a false indication of input amplitude. In many cases this might be due to short-lived noise spikes which become added to the input. For example, when scaled to accept a FS input of 1 V, the –80 dB level is only 100 µV, so when the mean input is only 60 dB below FS (1 mV), noise spikes of 0.9 mV are sufficient to cause momentary malfunction.

This effect can be minimized by using a simple low-pass filter ahead of the converter and a guard ring around the I_{IN} or $-V_{IN}$ pins. For a FS of 10 kHz a single-pole filter with a time-constant of 100 ms (Figure 2) will be suitable, but the optimum configuration will depend on the application and type of signal processing. Noise spikes are only likely to be a cause of error when the input current remains near its minimum value for long periods of time; above 100 nA (1 mV) full integration of additive input noise occurs.

The AD537 is somewhat susceptible to interference from other signals. The most sensitive nodes (besides the inputs) are the capacitor terminals and the SYNC pin. The timing capacitor should be located as close as possible to the AD537 to minimize signal pickup in the leads. In some cases, guard rings or shielding may be required. The SYNC pin should be decoupled through a 0.005 µF (or larger) capacitor to Pin 13 ($+V_S$). This minimizes the possibility that the AD537 will attempt to synchronize to a spurious signal. This precaution is unnecessary on the metal can package since the SYNC function is not brought out to a package pin and is thus not susceptible to pickup.

DECOUPLING

It is good engineering practice to use bypass capacitors on the supply-voltage pins and to insert small-valued resistors (10 Ω to 100 Ω) in the supply lines to provide a measure of decoupling between the various circuits in a system. Ceramic capacitors of 0.1 µF to 1.0 µF should be applied between the supply-voltage pins and analog signal ground for proper bypassing on the AD537.

A decoupling capacitor may also be useful from $+V_S$ to SYNC in those applications where very low cycle-to-cycle period variation (jitter) is demanded. By placing a capacitor across $+V_S$ and SYNC this noise is reduced. On the 10 kHz FS range, a 6.8 µF capacitor reduces the jitter to one in 20,000 which adequate for most applications. A tantalum capacitor should be used to avoid errors due to dc leakage.

NONLINEARITY SPECIFICATION

The preferred method for specifying linearity error is in terms of the maximum deviation from the ideal relationship after calibrating the converter at full scale and "zero". This error will vary with the full-scale frequency and the mode of operation. The AD537 operates best at a 10 kHz full-scale frequency with a negative voltage input; the linearity is typically within ±0.05%. Operating at higher frequencies or with positive inputs will degrade the linearity as indicates in the Specification table. The shape of a typical linearity plot is given in Figure 4.

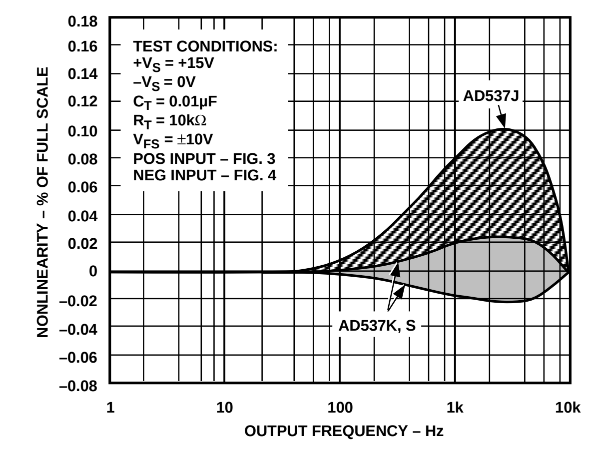


Figure 4a. Typical Nonlinearity Error Envelopes with 10 kHz F.S. Output

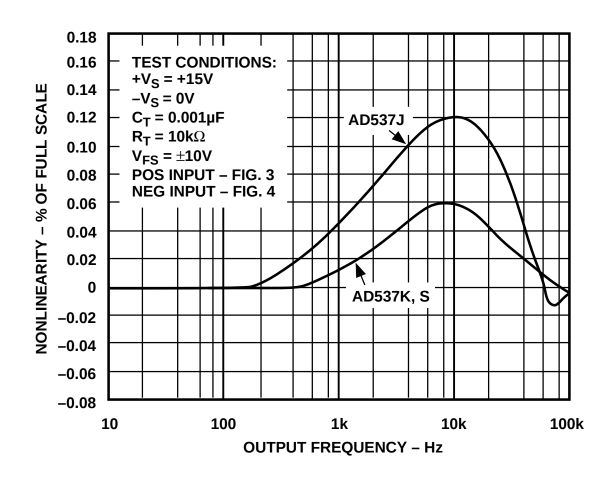
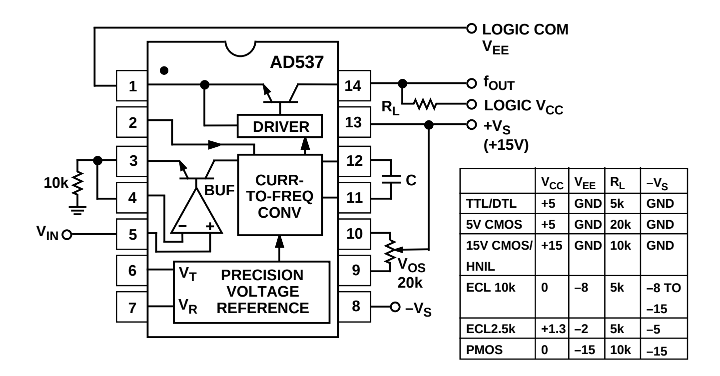


Figure 4b. Typical Nonlinearity Error with 100 kHz F.S. Output

OUTPUT INTERFACING CONSIDERATIONS

The design of the output stage allows easy interfacing to all digital logic families. The collector and emitter of the output NPN transistor are both uncommitted; the emitter can be tied to any voltage between $–V_S$ and 4 volts below $+V_S$. The open collector can be pulled up to a voltage 36 volts above the emitter regardless of $+V_S$. The high power output stage can supply up to 20 mA (10 mA for "H" package) at a maximum saturation voltage of 0.4 volts. The stage limits the output current at 25 mA; it can handle this limit indefinitely without damaging the device.

Figure 5 shows the AD537 with a standard 0 to +10 volt input connection and the output stage connections. The values for the logic common voltage, pull-up resistor, positive logic level, and $–V_S$ supply are given in the accompanying chart for several logic forms.



	V_{CC}	V_{EE}	R_L	$–V_S$
TTL/DTL	+5	GND	5k	GND
5V CMOS	+5	GND	20k	GND
15V CMOS/ HNIL	+15	GND	10k	GND
ECL 10k	0	–8	5k	–8 TO –15
ECL2.5k	+1.3	–2	5k	–5
PMOS	0	–15	10k	–15

Figure 5. Interfacing Standard Logic Families

APPLICATIONS

The diagrams and descriptions of the following applications are provided to stimulate the discerning engineer with alternative circuit design ideas. "Applications of the AD537 IC Voltage-to-Frequency Converter", available from Analog Devices on request, covers a wider range of topics and concepts in data conversion and data transmission using voltage-to-frequency converters.

TRUE TWO-WIRE DATA TRANSMISSION

Figure 6 shows the AD537 in a true two-wire data transmission scheme. The twisted-pair transmission lines serves the dual purpose of supplying power to the device and also carrying frequency data in the form of current modulation. The PNP circuit at the receiving end represents a fairly simple way for converting the current modulation back into a voltage square wave which will drive digital logic directly. The 0.6 volt square wave which will appear on the supply line at the device terminals does not affect the performance of the AD537 because of its excellent supply rejection. Also, note that the circuit operates at nearly constant average power regardless of frequency.

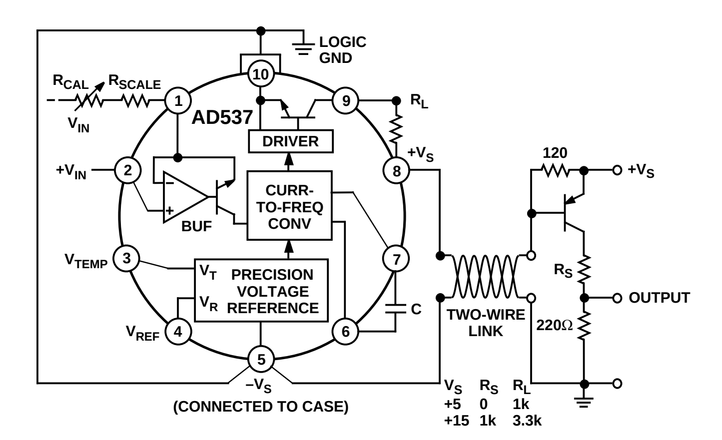


Figure 6. True Two-Wire Operation

F-V CONVERTERS

The AD537 can be used as a high linearity VCO in a phase-locked loop to accomplish frequency-to-voltage conversion. By operating the loop without a low-pass filter in the feedback path (first-order system), it can lock to any frequency from zero to an upper limit determined by the design, responding in three or four cycles to a step change of input frequency. In practice, the overall response time is determined by the characteristics of the averaging filter which follows the PLL.

Figure 7 shows a connection using a low power TTL quad open-collector nand gate which serves as the phase comparator. The input signal should be a pulse train or square wave with characteristics similar to TTL or 5-volt CMOS outputs. Any duty cycle is acceptable, but the minimum pulse width is 40 µs. The output voltage is one volt for a 10 kHz input frequency. The output as shown here is at a fairly high impedance level; for many situations an additional buffer may be required.

Trimming is similar to V-F application trimming. First set the V_{OS} trimmer to mid-scale. Apply a 10 kHz input frequency and trim the 2 kΩ potentiometer for 1.00 volts out. Then apply a 10 Hz waveform and trim the V_{OS} for 1 mV out. Finally, retrim the full-scale output at 10 kHz. Other frequency scales can be obtained by appropriate scaling of timing components.

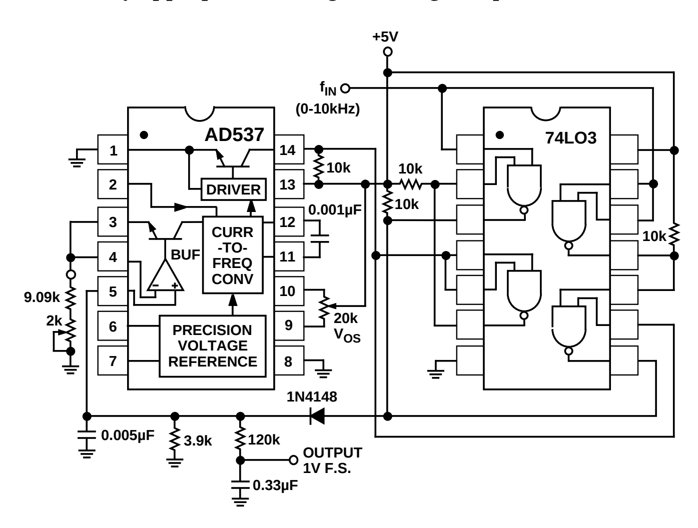


Figure 7. 10 kHz F-V Converter

TEMPERATURE-TO-FREQUENCY CONVERSION

The linear temperature-proportional output of the AD537 can be used as shown in these applications to perform various direct temperature-to-frequency conversion functions; it can also be used with other external connections in a temperature sensing or compensation scheme. If the sensor output is used externally, it should be buffered through an op amp since loading that point will cause significant error in the sensor output as well as in the main V-F converter circuitry.

An absolute temperature (Kelvin)-to-frequency converter is very easily accomplished, as shown in Figure 8. The 1 mV per K output serves as the input to the buffer amplifier, which then scales the oscillator drive current to a nominal 298 µA at +25°C (298K). Use of a 1000 pF capacitor results in a corresponding frequency of 2.98 kHz. Setting the single 2 kΩ trimmer for the correct frequency at a well-defined temperature near +25°C will normally result in an accuracy of ±2°C from –55°C to +125°C (using an AD537S). An NPO ceramic capacitor is recommended to minimize nonlinearity due to capacitance drift.

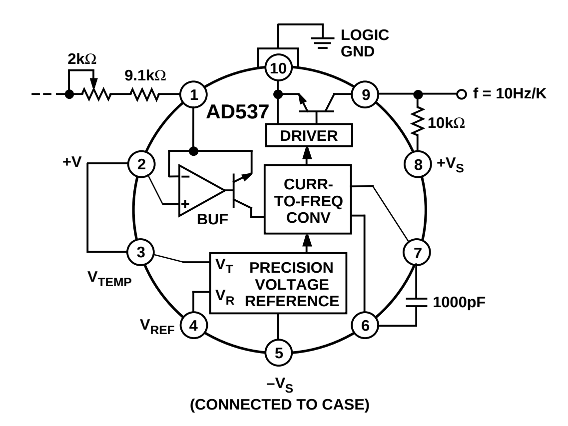


Figure 8. Absolute Temperature to Frequency Converter

OFFSET TEMPERATURE SCALES

Many other temperature scales can be set up by offsetting the temperature output with the voltage reference output. Such a scheme is shown by the Celsius-to-frequency converter in Figure 9. Corresponding component values for a Fahrenheit-to-frequency converter which give 10 Hz/°F are given in parentheses.

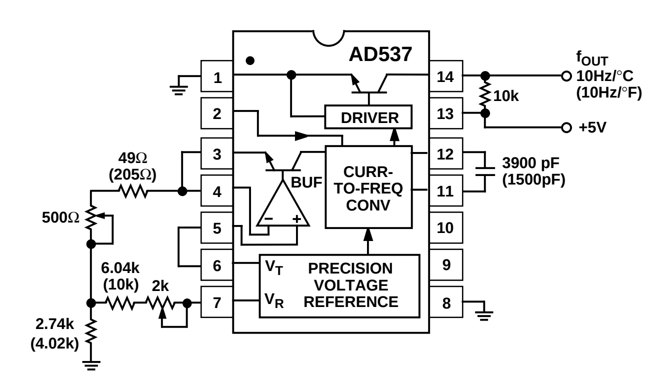


Figure 9. Offset Temperature Scale Converters Centigrade and (Fahrenheit) to Frequency

A simple calibration procedure which will provide ±2°C accuracy requires substitution of a 7.27k resistor for the series combination of the 6.04k with the 2k trimmer; then simply set the 500 Ω trimmer to give 250 Hz at +25°C.

High accuracy calibration procedure:

1. Measure room temperature in K.
2. Measure temperature output at Pin 6 at that temperature.
3. Calculate offset adjustment as follows:

$$Offset\ Voltage\ (mV) = \frac{V_{TEMP}\ (Pin\ 6)\ (mV)}{Room\ temp\ (K)} \times 273.2$$

4. Temporarily disconnect 49 Ω resistor (or 500 Ω pot) and trim 2 kΩ pot to give the offset voltage at the indicated node. Reconnect 49 Ω resistor.
5. Adjust slope trimmer to give proper frequency at room temperature (+25°C = 250 Hz).
   Adjustment for °F or any other scale is analogous.

SYNCHRONOUS OPERATION

The SYNC terminal at pin 2 of the DIP package can be used to synchronize a free running AD537 to a master oscillator, either at a multiple or a sub-multiple of the primary frequency. The preferred connection is shown in Figure 10. The diodes are used to produce the proper drive magnitude from high level signals. The SYNC terminal can also be used to shut off the oscillator. Shorting the terminal to $+V_S$ will stop the oscillator, and the output will go high (output NPN off).

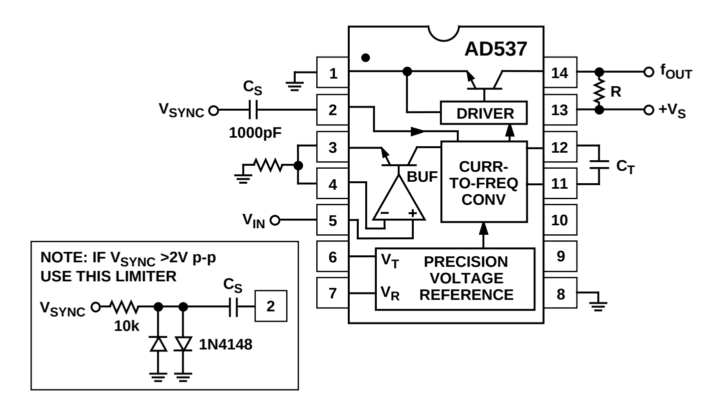


Figure 10. Connection for Synchronous Operation

Figure 11 shows the maximum pull-in range available at a given signal level; the optimum signal is a 0.8 to 1.0 volt square wave; signals below 0.1 volt will have no effect; signals above 2 volts p-p will disable the oscillator. The AD537 can normally be synchronized to a signal which forces it to a higher frequency up to 30% above the nominal free-running frequency, it can only be brought down about 1–2%.

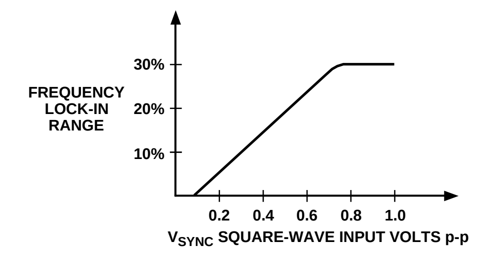


Figure 11. Maximum Frequency Lock-In Range vs. Sync. Signal

LINEAR PHASE LOCKED LOOP

The phase-locked-loop F/V circuit described earlier operates from an essentially noise-free binary input. PLL's are also used to extract frequency information from a noisy analog signal. To do this, the digital phase-comparator must be replaced by a linear multiplier. In the implementation shown in Figure 12, the triangular waveform appearing across the timing capacitor is used as one of the multiplier inputs; the signal provides the other input. It can be shown that the mean value of the multiplier output is zero when the two signals are in quadrature. In this condition, the ripple in the error signal is also quite small. Thus, the voltage at Pin 5 is essentially zero, and the frequency is determined primarily by the current in the timing resistor, controlled either manually or by a control voltage.

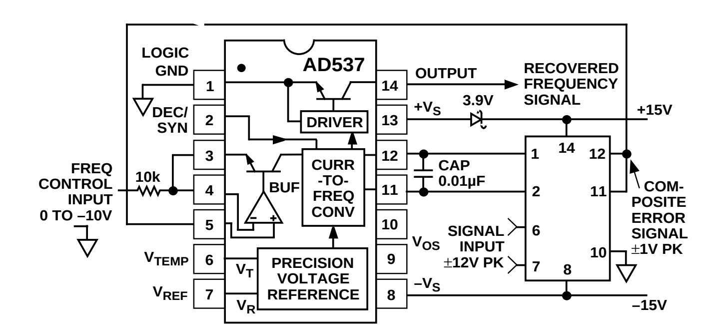


Figure 12. Linear Phase-Locked Loop

Noise on the input signal affects the loop operation only slightly; it appears as noise in the timing current, but this is averaged out by the timing capacitor. On the other hand, if the input frequency changes there is a net error voltage at Pin 5 which acts to bring the oscillator back into quadrature. Thus, the output at Pin 14 is a noise-free square-wave having exactly the same frequency as the input signal. The effectiveness of this circuit can be judged from Figure 13 which shows the response to an input of 1 V rms 1 kHz sinusoid plus 1 V rms Gaussian noise. The positive supply to the AD537 is reduced by about 4 V in order to keep the voltages at Pins 11 and 12 within the common-mode range of the AD534.

Since this is also a first-order loop the circuit possesses a very wide capture range. However, even better noise-integrating properties can be achieved by adding a filter between the multiplier output and the VCO input. Details of suitable filter characteristics can be found in the standard texts on the subject.

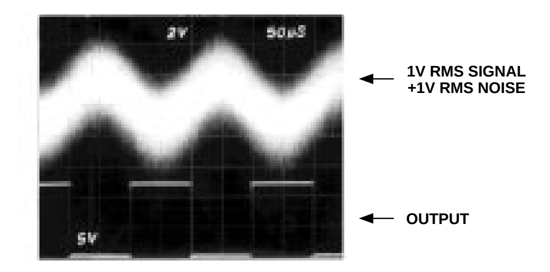


Figure 13. Performance of AD537 Linear Phase Locked Loop

By connecting the multiplier output to the lower end of the timing resistor and moving the control input to Pin 5, a high resistance frequency-control input is made available. However, due to the reduced supply voltage, this input cannot exceed +6 V.

TRANSDUCER INTERFACE

The AD537 was specifically designed to accept a broad range of input signals, particularly small voltage signals, which may be converted directly (unlike many V-F converters which require signal preconditioning). The 1.00 V stable reference output is also useful in interfacing situations, and the high input resistance allows nonloading interfacing from a source of varying resistance, such as the slider of a potentiometer.

THERMOCOUPLE INPUT

The output of a Chromel-Constantan (Type E) thermocouple, using a reference junction at 0°C, varies from 0 mV to 53.14 mV over the temperature range 0°C to +700°C with a slope of 80.678 μV/degree over most of its range and some nonlinearity over the range 0°C to +200°C. For this example, we assume that it is desired to indicate temperature in Degrees Celsius using a counter/display with a 100 ms gate width. Thus, the V-F converter must deliver an output of 7 kHz for an input of 53.14 mV. If very precise operation down to 0°C is imperative, some sort of linearizing is necessary (see, for example, *Analog Devices' Nonlinear Circuits Handbook*, pp. 92–97) but in many cases operation is only needed over part of the range.

The circuit shown in Figure 14 provides good accuracy from +300°C to +700°C. The extrapolation of the temperature voltage curve back to 0°C shows that an offset of –3.34 mV is required to fit the curve most exactly. This small amount of voltage can be introduced without an additional calibration step using the +1.00 V output of the AD537. To adjust the scale, the thermocouple should be raised to a known reference temperature near 500°C and the frequency adjusted to value using R1. The error should be within ±0.2% over the range 400°C to 700°C.

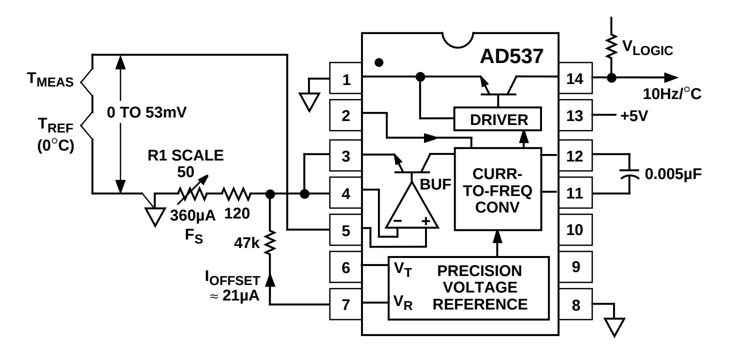
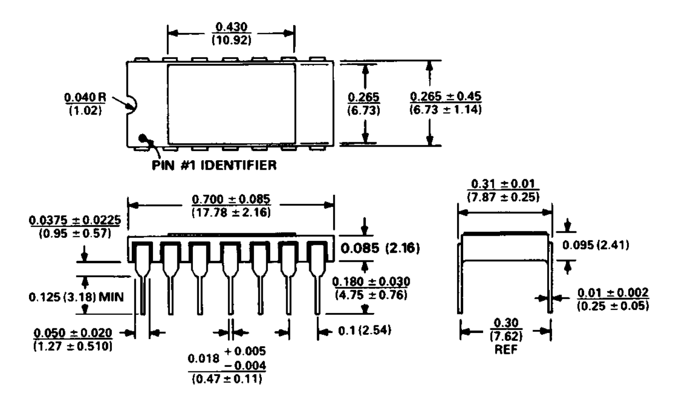


Figure 14. Thermocouple Interface with First-Order Linearization

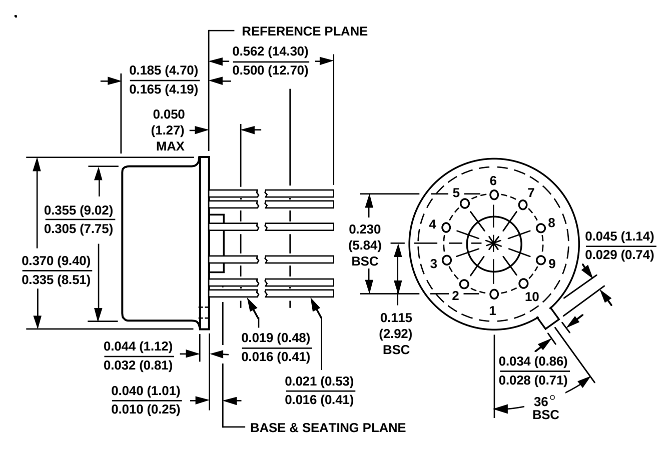
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

"D" Package – TO-116



"H" Package – TO-100



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